REMARKS

35 USC § 101

The Examiner has rejected claims 37 and 38 under 35 USC § 101 because the claimed invention is directed to non-statutory subject matter. Claims 37 and 38 have been amended to positively recite "a computer-readable storage device. . ." and accordingly the undersigned believes that the rejection of claims 37 and 38 under 35 USC § 101 is now overcome.

35 USC § 112

In the present invention, the delay times $t_1,..., t_N$ are proportional to values $u_1,..., u_N$, respectively and the values $u_1,..., u_N$ are computed by

- a prestored integer `a',
- a predetermined nonlinear transformation 'f(·)', and
- recurrence equations:

$u_1 = a;$

$u_{j+1} = f(u_j)$ $(1 \leq j < N)$,

and the proportionally coefficient `C' is computed so that the delay times $t_1,..., t_N$ are shorter than the reciprocal number of a minimum value of clock rates of the multiple input received synchronized signals $r_1, ..., r_N$,

$t_1 = C\, u_1,$

$t_2 = C\, u_2,$

...,

$t_N = C\, u_N.$

For example, in the filed of CDMA communication, a random number included in a random number sequence that forms a spreading code is superimposed on a transmission signal one value for 1 clock (1 chip), and the superimposed value is transmitted.

In the case where, for example, the information is superimposed by a spreading code comprising L number of symbols in transmission thereof, L clock period (L chip length, L symbol length) of time is required.

The prior art teaches synchronizing clocks of signals when communication is performed by using a plurality of signals.

On the other hand, in the present invention, the clock of each signal is displaced from a reference clock by $t_1,..., t_N$ in transmission and reception thereof.

The length of displacement is determined by nonlinear transformation.

The transmitter and the receiver use a common $t_1,..., t_N$, , and the transmission side positively displaces clock/chip of each signal and the reception side displaces the time to cancel the amount displaced at the transmission side, in the opposite direction.

Furthermore, the time displacement of each signal is determined by non-linear conversion. By adopting such a configuration, it becomes possible to further ensure the separation of each signal.

The Examiner stated that "it seems like by doing so some data is lost since the delay amount is less than the maximum of clock period of the multiple input signals". However, the processing is performed after that a reception signal a_i is delayed by a time $T - t_i$ from the reference clock to cancel the delay time at the transmission side, in synchronization with the transmission of a transmission signal w_i delayed by a time t_i from the reference clock, synchronized with other signals, and a synchronized signal p_i is obtained.

Therefore, even if the delay amount is less than the maximum of clock period of multiple input signals, data will not be lost.

Further, since the signal $r_1,..., r_N$ in the present application is a synchronization signal, the clock rate is common, the reciprocal number of the minimum value of clock rates is equal to the clock period (chip length, reciprocal number of symbol rate).

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Any fee due with the filing of this response may be charged to our Deposit Account No. 50-3145, under Order No. 215384-101174 from which the undersigned is authorized to draw.

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Respectfully submitted,

By _____
Joseph V. Coppola, Sr.
Registration No.: 33,373
HONIGMAN MILLER SCHWARTZ AND COHN LLP
38500 Woodward Avenue
Suite 100
Bloomfield Hills, Michigan 48304-5048
(248) 566-8500
Attorney for Applicant